32-Channel Serial to Parallel Converter With Open Drain Outputs

Features

- Processed with HVCMOS® technology
- Output voltages to 225V using a ramped supply voltage
- SINK current minimum 100mA
- Shift register speed 8.0MHz
- Strobe and enable inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Hi-Rel processing available

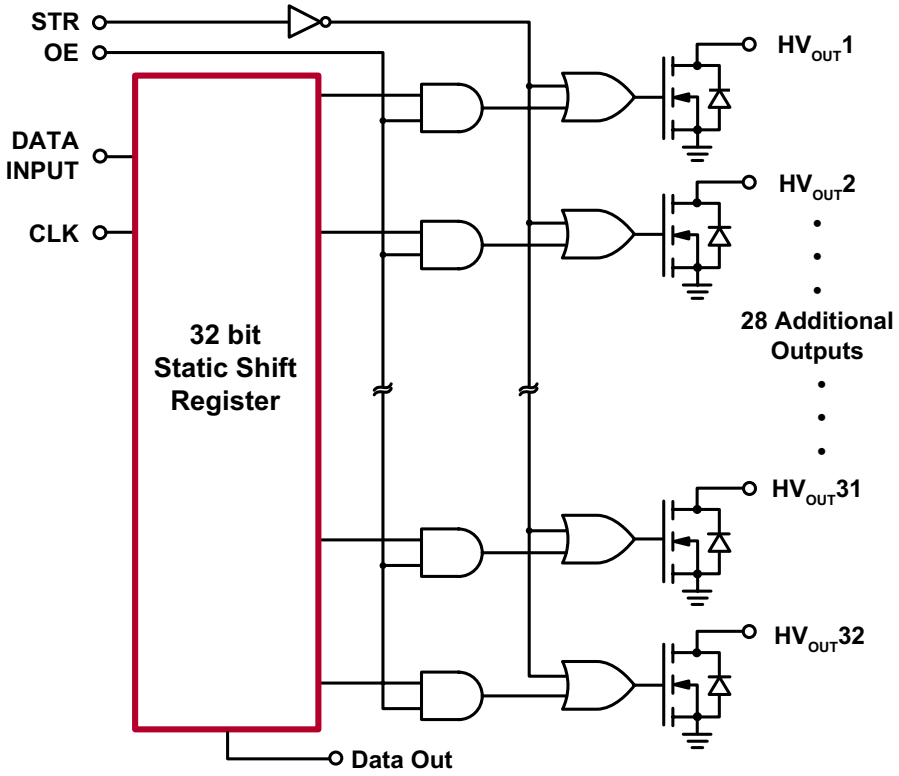
General Description

The HV5222 is a low voltage serial to high voltage parallel converter with open drain outputs. This device has been designed for use as a driver for AC electroluminescent displays.They can also be used in any application requiring multiple output high voltage current sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent, or large matrix LCD displays.

This device consists of a 32-bit shift register and control logic to perform the Output Enable and all-on functions. Data is shifted through the shift register on the high to low transition of the clock. The HV5222 shifts in the clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the OE(Output Enable) or the STR (Strobe) inputs.

The HV5222 has been designed to be used in systems which either switch off the high voltage supply before changing the state of the high voltage outputs or which limit the current through each output.

Functional Block Diagram



Ordering Information

Part Number	Package	Packing
HV5222DJ-G*	44-Lead Quad Cerpac	27/Tube
HV5222PG-G	44-Lead PQFP	96/Tray
HV5222PG-G M919	44-Lead PQFP	500/Reel
HV5222PJ-G	44-Lead PLCC	27/Tube
HV5222PJ-G M903	44-Lead PLCC	500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package
** Hi-Rel processing available*

Absolute Maximum Ratings

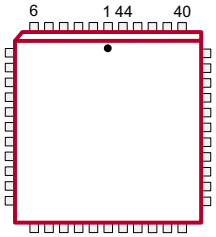
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +15V
Supply voltage, V_{PP}	-0.5V to +250V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[1]	1.5A
Continuous total power dissipation[2] Plastic Ceramic	 1200W 1500W
Operating temperature range Plastic Ceramic	 -40°C to +85°C -55°C to +125°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

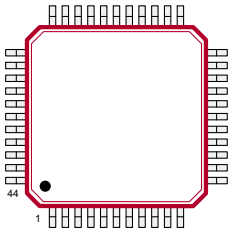
Notes:

1. *Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.*

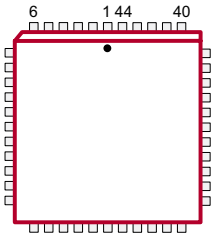
Pin Configuration



44-Lead Quad Cerpac Chip Carrier



44-Lead Quad Plastic Gullwing



44-Lead Quad Plastic Chip Carrier

Typical Thermal Resistance

Package	θ_{ja}
44-Lead Quad Cerpac	---
44-Lead PQFP	51°C/W
44-Lead PLCC	37°C/W

Product Marking

Top Marking

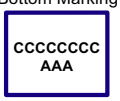
Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
**May be part of top marking*

44-Lead Quad Cerpac Chip Carrier

Top Marking

Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

44-Lead Quad Plastic Gullwing

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*
____ = "Green" Packaging
**May be part of top marking*

44-Lead Quad Plastic Chip Carrier

Packages may or may not include the following marks: Si or 

Recommended Operating Conditions

Sym	Parameter		Min	Typ	Max	Units
V_{DD}	Logic voltage supply		10.8	12	13.2	V
HV_{OUT}	High voltage output		-0.3	-	225	V
V_{IH}	High-level input voltage		V_{DD} -2.0	-	V_{DD}	V
V_{IL}	Low-level input voltage		0	-	2.0	V
f_{CLK}	Clock frequency		-	-	8.0	MHz
T_A	Operating free-air temperature	Plastic	-40	-	+85	°C
		Ceramic	-55	-	+125	

Power-Up Sequence

Power-up sequence should be the following:

1. *Connect ground*
2. *Apply V_{DD}*
3. *Set all inputs to a known state*

Power-down sequence should be the reverse of the above.

Electrical Characteristics *(Over recommended operating conditions unless otherwise specified)*

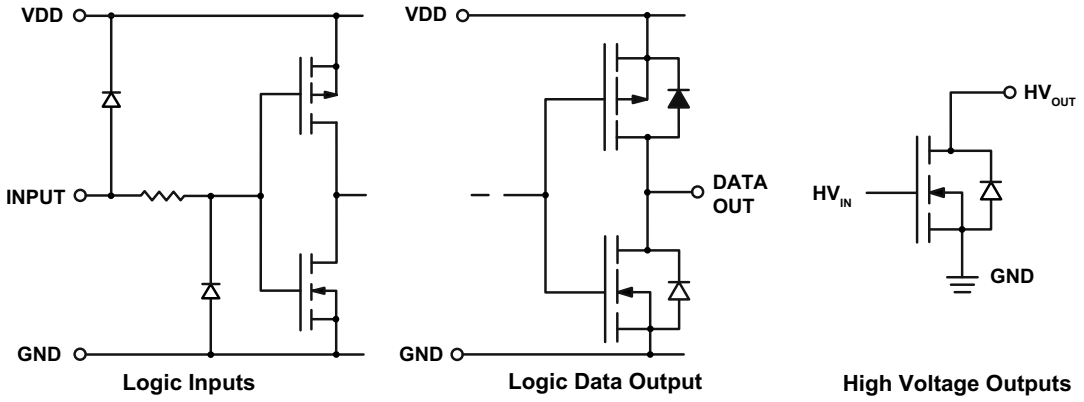
DC Characteristics

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	15	mA	f_{CLK} = 8.0MHz, F_{DATA} = 4.0MHz
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All V_{IN} = 0V
$I_{O(OFF)}$	Off-state output current		-	10	µA	All outputs high, all SWS parallel
I_{IH}	High level logic input current		-	1.0	µA	V_{IH} = 12V
I_{IL}	Low level logic input current		-	-1.0	µA	V_{IL} = 0
V_{OH}	High level output data out		V_{DD} -1.0V	-	V	I_{DOUT} = -100µA
V_{OL}	Low level output voltage	HV_{OUT}	-	15	V	I_{HVOUT} = +100mA
		Data out	-	1.0		I_{DOUT} = +100µA
V_{OC}	HV_{OUT} clamp voltage		-	-1.5	V	I_{OL} = -100mA

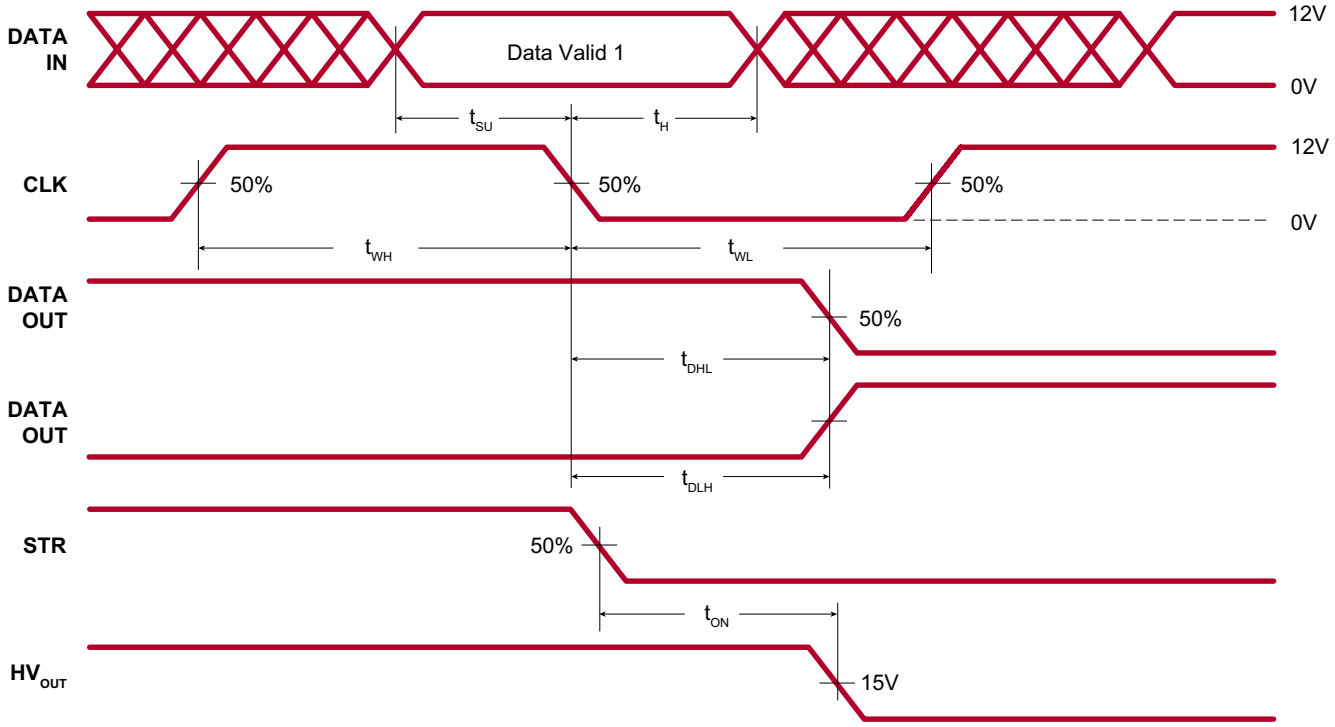
AC Characteristics *(V_{DD} = 12V, T_A = 25°C)*

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	---
t_W	Clock width, high or low	62	-	ns	---
t_{SU}	Data setup time before CLK falls	25	-	ns	---
t_H	Data hold time after CLK falls	10	-	ns	---
t_{ON}	Turn-on time, HV_{OUT} from strobe	-	500	ns	R_L = 2.0KΩ to 200V
t_{DHL}	Data output delay after H to L CLK	-	100	ns	C_L = 15pF
t_{DLH}	Data output delay after L to H CLK	-	100	ns	C_L = 15pF

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs				Outputs				
	Data In	CLK	OE	Strobe	Shift Reg		HV Outputs		Data Out
					1	2...32	1	2...32	
All on	X	X	X	L	●	●...●	ON	ON...ON	●
All off	X	X	L	H	●	●...●	OFF	OFF...OFF	●
Load S/R	H OR L	↓	L	H	H or L	●...●	OFF	OFF...OFF	-
Output Enable	X	H OR L	H	H	H or L	●...●	ON or OFF	●...●	●

Notes:

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

● = dependent on previous stage's state before the last CLK: High-to-low transition

44-Lead PQFP Pin Description

Pin	Function	Description
1	$HV_{OUT}22$	High voltage outputs.
2	$HV_{OUT}21$	
3	$HV_{OUT}20$	
4	$HV_{OUT}19$	
5	$HV_{OUT}18$	
6	$HV_{OUT}17$	
7	$HV_{OUT}16$	
8	$HV_{OUT}15$	
9	$HV_{OUT}14$	
10	$HV_{OUT}13$	
11	$HV_{OUT}12$	
12	$HV_{OUT}11$	
13	$HV_{OUT}10$	
14	$HV_{OUT}9$	
15	$HV_{OUT}8$	
16	$HV_{OUT}7$	
17	$HV_{OUT}6$	
18	$HV_{OUT}5$	
19	$HV_{OUT}4$	
20	$HV_{OUT}3$	
21	$HV_{OUT}2$	
22	$HV_{OUT}1$	
23	DATA OUT	Serial data output Data output for cascading to the data input of the next device.
24	N/C	No connect.
25		
26		
27		
28	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
29	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.
30	GND	Logic and high voltage ground.
31	VDD	Low voltage logic power rail.
32	STR	Strobe.
33	DATA IN	Serial data input Data needs to be present before each rising edge of the clock.

44-Lead PQFP Pin Description *(cont.)*

Pin	Function	Description
34	N/C	No connect
35	$HV_{OUT}32$	High voltage outputs.
36	$HV_{OUT}31$	
37	$HV_{OUT}30$	
38	$HV_{OUT}29$	
39	$HV_{OUT}28$	
40	$HV_{OUT}27$	
41	$HV_{OUT}26$	
42	$HV_{OUT}25$	
43	$HV_{OUT}24$	
44	$HV_{OUT}23$	

44-Lead PLCC Pin Description

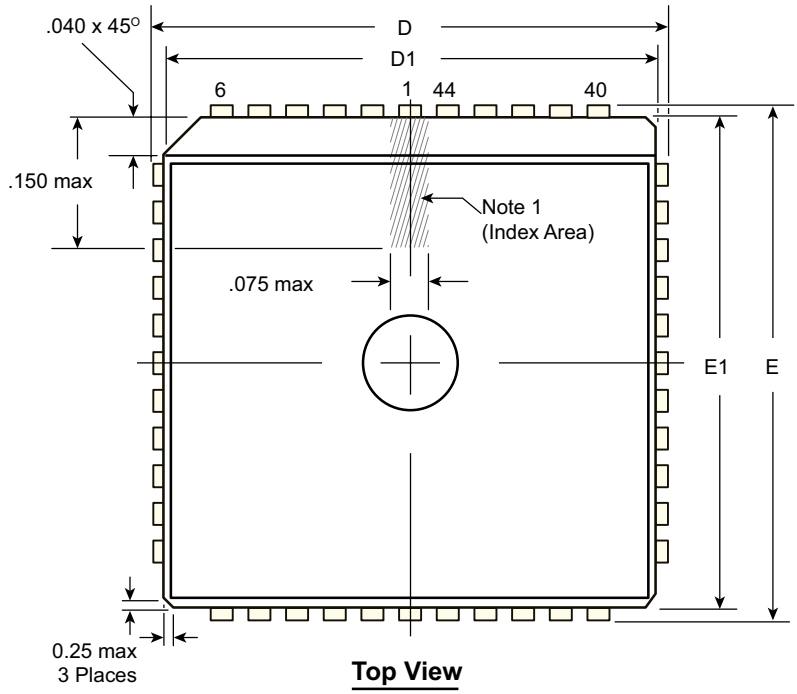
Pin	Function	Description
1	$HV_{OUT}17$	High voltage outputs.
2	$HV_{OUT}16$	
3	$HV_{OUT}15$	
4	$HV_{OUT}14$	
5	$HV_{OUT}13$	
6	$HV_{OUT}12$	
7	$HV_{OUT}11$	
8	$HV_{OUT}10$	
9	$HV_{OUT}9$	
10	$HV_{OUT}8$	
11	$HV_{OUT}7$	
12	$HV_{OUT}6$	
13	$HV_{OUT}5$	
14	$HV_{OUT}4$	
15	$HV_{OUT}3$	
16	$HV_{OUT}2$	
17	$HV_{OUT}1$	
18	DATA OUT	Serial data output Data output for cascading to the data input of the next device.

44-Lead PLCC Pin Description *(cont.)*

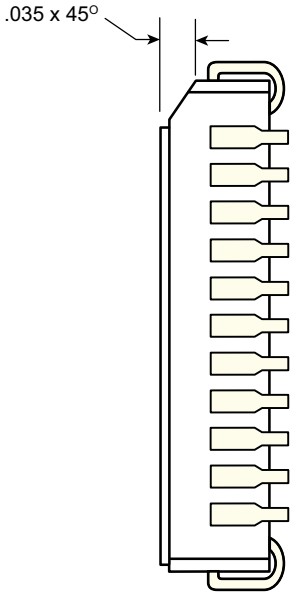
Pin	Function	Description
19	N/C	No connect.
20		
21		
22		
23	OE	Output enable input. When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched.
24	CLK	Data shift register clock. Input are shifted into the shift register on the positive edge of the clock.
25	GND	Logic and high voltage ground.
26	VDD	Low voltage logic power rail.
27	STR	Strobe.
28	DATA IN	Serial data input Data needs to be present before each rising edge of the clock.
29	N/C	No connect
30	$HV_{OUT}32$	High voltage outputs.
31	$HV_{OUT}31$	
32	$HV_{OUT}30$	
33	$HV_{OUT}29$	
34	$HV_{OUT}28$	
35	$HV_{OUT}27$	
36	$HV_{OUT}26$	
37	$HV_{OUT}25$	
38	$HV_{OUT}24$	
39	$HV_{OUT}23$	
40	$HV_{OUT}22$	
41	$HV_{OUT}21$	
42	$HV_{OUT}20$	
43	$HV_{OUT}19$	
44	$HV_{OUT}18$	

44-Lead Quad Cerpac Package Outline (DJ)

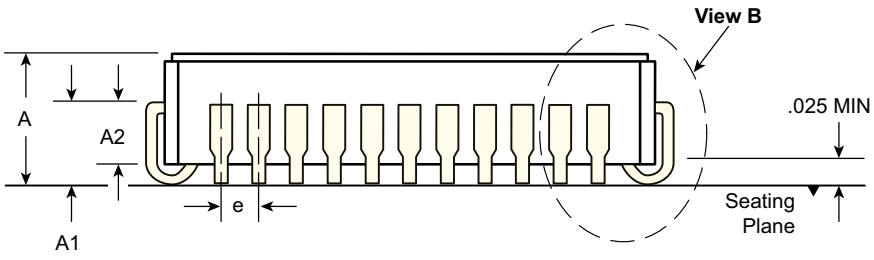
.650x.650in body, .190in height (max), .050pin pitch



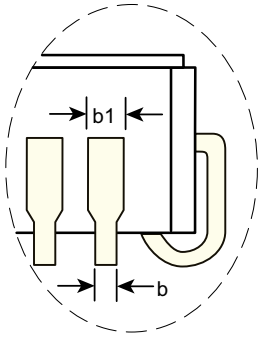
Top View



Vertical Side View



Horizontal Side View



View B

Note:

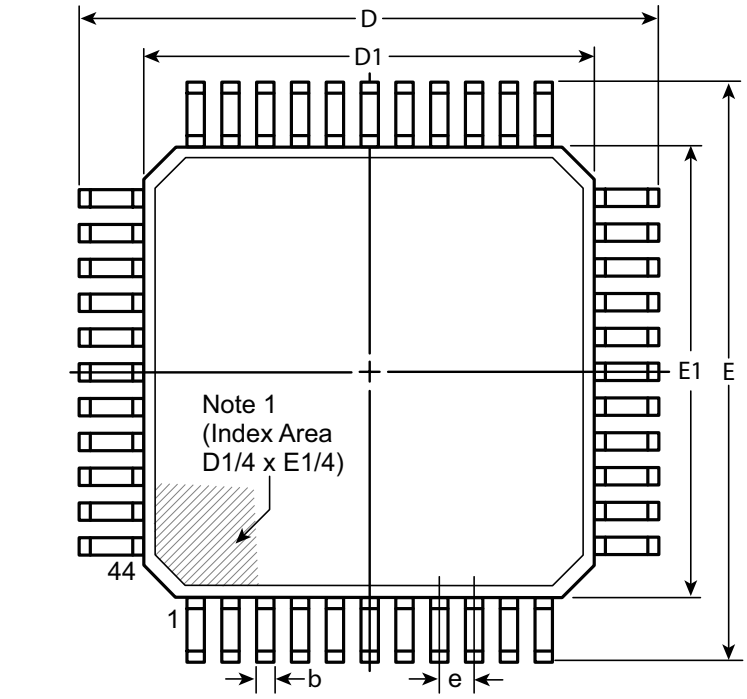
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.155	.090	.060 REF	.017	.026	.685	.630	.685	.630	.050 BSC
	NOM	.172	.100		.019	.029	.690	.650	.690	.650	
	MAX	.190	.120		.021	.032	.695	.665	.695	.665	

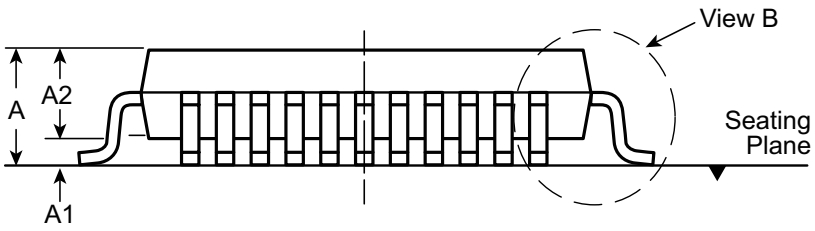
JEDEC Registration MO-087, Variation AB, Issue B, August, 1991.
Drawings not to scale.
Supertex Doc. #: *DSPD-44CERPACDJ, Version D090808.*

44-Lead PQFP Package Outline (PG)

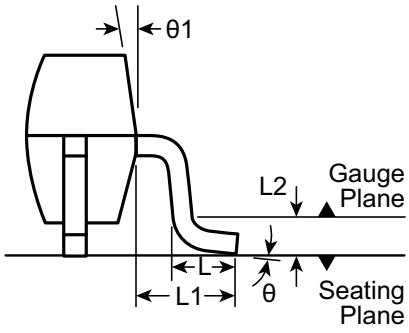
10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Top View



Side View



View B

Note:

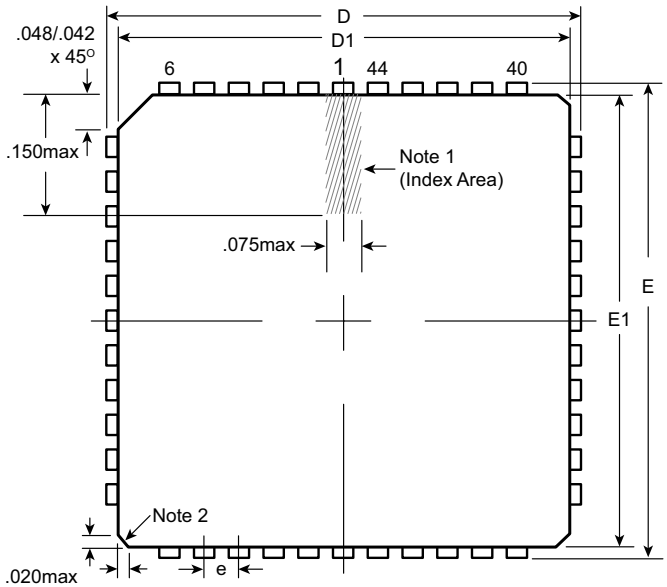
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

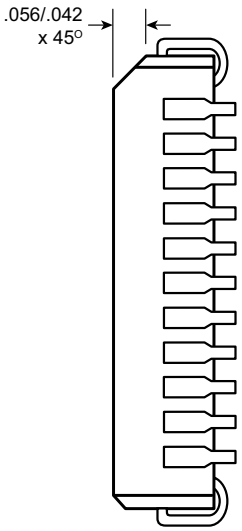
JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex** Doc. #: DSPD-44PQFPPG, Version C041309.*

44-Lead PLCC Package Outline (PJ)

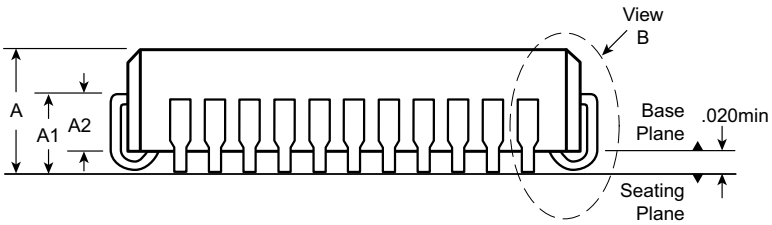
.653x.653in body, .180in height (max), .050pitch



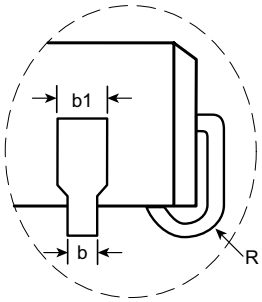
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44PLCCPJ, Version F031111.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to: http://www.supertex.com/packaging.html.)

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